Shrirang (Arvind) K. Karandikar

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Experience

April 2018 – present	AlgoAsylum Founder

AlgoAsylum is a platform for cross-disciplinary collaborations in the digitalization space. *Activities* include consulting, training and incubation on digitalization *technologies* such as HPC, AI, Blockchain, Robotics and IoT for *participants* who are domain experts, technology experts, corporations large and small, and startups.

Multiple interesting projects with students are in progress. 2 patents have been filed, we have won hackathons and other competitions and multiple publications are in the pipeline. I have also been awarded an Emergent Ventures grant for my work on hyper-local pollution monitoring.

February 2021 – present	Cummins College of Engineering for Women Adjunct Professor of Electronics and Telecommunication
June 2022 – present	MIT World Peace University Adjunct Professor of Petroleum Engineering
November 2012 – April 2018	Shell India Markets Pvt. Ltd. General Manager, Computational Technology

I built up and led a global team evaluating new technologies and developments in existing computational methods (machine learning, cloud, blockchain, HPC) and applying these within Shell. I interfaced with stakeholders across multiple business units and geographies.

My responsibilities included setting strategy, capability build, team and stakeholder management, budget allocation and management, and value-based delivery.

June 2007 – June 2012	Computational Research Labs, India Distinguished Scientist and Group Head, Technology Innovation

I directed all research in hardware, software and system design, with focus on high performance computing, parallel algorithms and efficient implementations. This was achieved through a team I built up from scratch. I also interfaced with external customers and supported commercial activities.

CRL developed EKA, India's first supercomputer ranked #4 on the Top500 list of supercomputers, 2008. To date, this has been the highest rank of any Indian supercomputer on the Top500 list.

January 2005 – May 2007	IBM Austin Research Labs Research Staff Member

I was the principal developer of EVE (Electrical Violation Eliminator), an approach for electrical correction that was (at that time) more effective, significantly faster and used less overhead than previous methods. My work influenced related areas such as buffering and gate sizing, and drove further development of methodology flows in PDS, IBM's principal tool for physical design.

This work resulted in 5 patents and multiple publications in the area of VLSI physical design and optimization.

January 1997 – September 1999	Intel Corp. Component Design Engineer

I worked on the design and development of SHARK-FG, a switch level fault simulator. My contribution involved parallelizing the tool, enabling the simulation of multi-million transistor designs (which was not possible on single machines at the time). This tool was used for evaluating test vectors for the Itanium microprocessor, significantly reducing tester time.

I worked on the design and development of AutoCov, a genetic-programming based tool for improving test coverage. I owned and was responsible for the test evaluator, which determined the "fitness" of current tests, and directing the generation of new tests. AutoCov was used in developing the test suite for the Pentium-4 series of microprocessors.

September 1994 – August 1995	Senior Sales Engineer, NIIT Ltd.

I was the marketing lead for Mentor Graphics(EDA) and Arc/Info(GIS) software packages in India. I was responsible for educating users on the need for automation and the quality of our solution package. This was at a time when the computer revolution was yet to take off in India, and the marked for EDA and GIS software had to be created from scratch.

Education

Doctor of Philosophy, Electrical Engineering
Minors: Mathematics, Computer Science
Thesis: Synthesis and Performance Prediction of VLSI Designs
University of Minnesota
2004

Master of Science, Electrical Engineering
Thesis: CAD Algorithms for VLSI Physical Design
Clarkson University
1996

Bachelor of Engineering, Electronics and Telecommunications
University of Pune
1994

Diploma in Advanced Computing
Advanced Computing Training School, C-DAC
1994

Publications

Conference Publications

[1] Arvind K. Karandikar, Peichen Pan, and C. L. Liu. Optimal Clock Period Clustering for Sequential Circuits with Retiming. In *Proceedings of the IEEE International Conference on Computer Design*, pages 122-127, 1997.

[2] Shrirang K. Karandikar and Sachin S. Sapatnekar. Technology Mapping for SOI Domino Logic Incorporating Solutions for the Parasitic Bipolar Effect. In *Proceedings of the IEEE/ACM Design Automation Conference*, pages 377-382, 2001.

[3] Shrirang K. Karandikar and Sachin S. Sapatnekar. Fast Comparisons of Circuit Implementations. In *Proceedings of the Design, Automation and Test in Europe Conference*, pages 910-915, 2004.

[4] Shrirang K. Karandikar and Sachin S. Sapatnekar. Logical Effort Based Technology Mapping. In *Proceedings of the IEEE/ACM International Conference on Computer Aided Design*, pages 419-422, 2004.

[5] Shrirang K. Karandikar and Sachin S. Sapatnekar. Fast Estimation Of Area-Delay Tradeoffs In Circuit Sizing. In *Proceedings of the IEEE International Symposium on Circuits And Systems*, pages 3575--3578, 2005.

[6] Shiyan Hu, Charles J. Alpert, Jiang Hu, Shrirang K. Karandikar, Zhuo Li, Weiping Shi and C.-N. Sze. Fast Algorithms for Slew Constrained Minimum Cost Buffering. In *Proceedings of the IEEE/ACM Design Automation Conference*, pages 308--313 2006.

[7] Shrirang K. Karandikar, Charles J. Alpert, Mehmet C. Yildiz, Paul Villarrubia, Stephen T. Quay, Tuhin Mahmud. Fast Electrical Correction Using Resizing and Buffering. In *Proceedings of the IEEE/ACM Asia-South Pacific Design Automation Conference*, pages 553--558,2007.

[8] Charles J. Alpert, Shrirang K. Karandikar, Zhuo Li, Gi-Joon Nam, Stephen T. Quay, Haoxing Ren, Cliff Sze, Paul Villarrubia, Mehmet C. Yildiz. The Nuts and Bolts of Physical Synthesis. In *Proceedings of the 2007 International Workshop on System Level Interconnect Prediction*, pages 89--94,2007.

[9] A. K. Agrawal, C. Bhattacharya, Prakalp Somawanshi, Mahesh Khadtare and Shrirang K. Karandikar Accelerated SAR Image Generation on GPGPU. In *Proceedings of the 3rd Asia-Pacific Conference on Synthetic Aperture Radar* , pages 371--374, 2011.

[10] Varad R. Deshmukh and Nishchay S. Mhatre and Shrirang K. Karandikar FIRA - A Novel Method for Benchmarking the Cache Hierarchy. In *Proceedings of ACM COMPUTE 2012* , pages --,2012.

Journal Publications

[1] Peichen Pan, Arvind K. Karandikar, and C. L. Liu. Optimal Clock Period Clustering for Sequential Circuits with Retiming. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 17(6):489-498, June 1998.

[2] Shrirang K. Karandikar and Sachin S. Sapatnekar. Technology Mapping for SOI Domino Logic Incorporating Solutions for the Parasitic Bipolar Effect. *IEEE Transactions on VLSI Systems*, 11(6):1094-1105, December 2003.
Also see Erratum. *IEEE Transactions on VLSI Systems*, 12(6):669-670, June 2004.

[3] Shrirang K. Karandikar and Sachin S. Sapatnekar. Fast Comparisons of Circuit Implementations. *IEEE Transactions on VLSI Systems*, 13(12):1329--1339, December 2005.

[4] Charles J. Alpert, Shrirang K. Karandikar, Zhuo Li, Gi-Joon Nam, Stephen T. Quay, Haoxing Ren, C.-N. Sze, Paul G. Villarrubia and Mehmet Yildiz. Techniques for Fast Physical Synthesis. *Proceedings of the IEEE*, 95(3):573--579, March 2007.

[5] Shiyan Hu, Charles J. Alpert, Jiang Hu, Shrirang K. Karandikar, Zhuo Li, Weiping Shi and Chin-Ngai Sze. Fast Algorithms For Slew Constrained Minimum Cost Buffering. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 26(11):2009--2022, November 2007.

[6] Shrirang K. Karandikar and Sachin S. Sapatnekar. Technology Mapping Using Logical Effort Solving the Load Distribution Problem. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 27(1):45--58, January 2008.

Invited Talks, Presentations and Workshops (without proceedings)

[1] Shrirang K. Karandikar and Sachin S. Sapatnekar. Extending Logical Effort for Fast Comparisons of Circuit Implementations. *SRC TECHCON*, August 2003.

[2] Shrirang K. Karandikar. A Quick Introduction to LaTeX. *Twin Cities Linux Users Group*, Monthly Meeting, February 2004.

[3] P. Kudva, B. Curran, S. K. Karandikar, M. Mayo, S. Carey and S. S. Sapatnekar. Early Performance Prediction. In *Workshop on Complexity-Effective Design*, 2005.

[4] Shrirang K. Karandikar, Charles J. Alpert, Mehmet C. Yildiz, Paul G. Villarrubia, Stephen T. Quay and Tuhin Mahmud. Fast Electrical Correction Using Resizing and Buffering. In *International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, 2006

[5] Shiyan Hu, Charles J. Alpert, Jiang Hu, Shrirang K. Karandikar, Zhuo Li, Weiping Shi and Chin-Ngai Sze. Fast Algorithms for Slew Constrained Minimum Cost Buffering. In *7th International Austin CAS Conference*, 2006

[6] C. J. Alpert, S. K. Karandikar *et al*. The Mercury Flow -- Integrating PLATO into High-Effort PDS. In *IBM Design Automation Workshop*, 2006.

[7] Shrirang K. Karandikar, Chin-Ngai Sze *et al*. EVE -- Electrical Violation Eliminator. In *IBM Design Automation Workshop*, 2006.

[8] Shrirang K. Karandikar, S. K. Dash and S. Rai. Regional Climate Modelling and High Performance Computation. In *First Annual Workshop on Climate Modelling*, 2008.

[9] Shrirang K. Karandikar. High Performance Computing Solutions at CRL. In *ATIP First Workshop on HPC in India: Indigenous Hardware, Software, and Infrastructure Research*, 2009.

[10] Shrirang K. Karandikar, Kiran Nalawade and Sandip Tikkar. Performance Optimization. In *IEEE International Conference on High Performance Computing*, 2009.

[11] Shrirang K. Karandikar. CRL's Experiments and Experiences with Grid and Cloud. In *GARUDA-NKN Partners Meet*, 2011.

[12] Shrirang K. Karandikar. From Cycles to Solutions. In *International Conference on Frontiers of Computer Science*, 2011.

[13] Nitin Joshi, Shashank Srivastava, Milner Kumar, Jojumon Kavalan, Shrirang K. Karandikar and Arundhati Saraph. Parallelization of Velvet, A de-novo Genmone Sequence Assembler. In *IEEE International Conference on High Performance Computing*, 2011.

[14] Varad R. Deshmukh and Nishchay S. Mhatre and Shrirang K. Karandikar. Techniques for Benchmarking CPU Microarchitecture for Performance Evaluation. In *IEEE International Conference on High Performance Computing*, 2011.

[15] Shrirang K. Karandikar. High Performance Computing and the Cloud. In *Challenges in Cloud Computing, DIAT Pune*, 2011.

[16] Nitin Gavhane, Shrirang K. Karandikar, Biswajit Mishra, Prakalp Somawanshi and Murthy Udupa, Performance Analysis and Optimization of HPC Applications, In *Subsurface and Wells Software Developer's Summit*, 2013.

[17] Prakrati Agrawal, Yashodhan Karandikar and Shrirang K. Karandikar. Quick(er)Sort. *In IISc Summer School*, 2014.

[18] Shrirang K. Karandikar, Suchismita Sanyal and Praveen Pankajakshan. Accelerating Materials Design. In *Intel DevCloud Summit*, 2018.

[19] Shrirang K. Karandikar. Putting the Smart in SmartGrids. In *IoT, AI and Blockchain for Smart Grids, India Smart Utility Week*, 2019

[20] Siddharth Srivastava, Yash Damania, Yash Choudhari, Raghav Gaggar, and Shrirang K. Karandikar. The View from Above: Getting Started with Satellite Images. In *PyCon India* 2020.

[21] Abhishek Deshpande, Soham Joshi, Varad Deshmukh and Shrirang K. Karandikar. Understanding UMAP: The Internal Workings of a State-of-the-Art Clustering Algorithm. In *PyCon India* 2020.

[22] Soham Joshi, Abhishek Deshpande, Varad Deshmukh and Shrirang K. Karandikar. Modeling Pandemics. In *Intel AI Summit*, 2020

Patents

[1] Shrirang K. Karandikar, Charles J. Alpert, Mehmet C. Yildiz, Stephen T. Quay, Tuhin Mahmud and Paul G. Villarrubia. EVE: Electrical Violation Eliminator. IBM Invention Disclosure AUS8-2005-1486, August 2005.

[2] Charles J. Alpert, Shrirang K. Karandikar, Tuhin Mahmud, Stephen T. Quay and Chin-Ngai Sze. Slew Constrained Minimum Cost Buffering. U. S. Patent 7,448,007, issued November 2008.

[3] Charles J. Alpert, Shrirang K. Karandikar, Tuhin Mahmud, Stephen T. Quay and Chin-Ngai Sze. Slew Constrained Minimum Cost Buffering. U. S. Patent 7,890,905, issued February 2011.

[4] Zhuo Li, Charles J. Alpert, Cliff Sze, and Shrirang K. Karandikar. Placement Congestion Driven Node Cost Model for Buffer Insertion. IBM Invention Disclosure AUS8-2006-1392, October 2006.

[5] David A. Papa, Charles J. Alpert, Gi-Joon Nam, Arvind K. Karandikar, Zhuo Li, Chin-Ngai Sze. A Method To Improve the Timing of A Circuit by Moving Badly Placed Gates. IBM Invention Disclosure AUS8-2007-0328, February 2007.

[6] Kimaya Badhe, Neha Chaudhari, Samruddhi Kanhed, Kanchan Sarolkar, Arvind K. Karandikar. System and Method for Optimization of Reading Performance Using Character and Fonts. Provisional application number 201921030947, July 2019.

[7] Kimaya Badhe, Neha Chaudhari, Samruddhi Kanhed, Kanchan Sarolkar, Sakshi Mandke, Arvind K. Karandikar. System for Individual Identification based on Eye-tracking and methods thereof. Provisional application number 202121025718, June 2021.

Other Activities

Multiple contributions to curriculum development and mulitple universities and colleges.

Judge / Evaluator at AICTE competitions (Smart India Hackathon, Toycathon) and college innovation competitions.

Evaluator for undergraduate and graduate final year projects.

Guest lecturer for specialized topics in VLSI design, AI/ML and HPC.