

# Shrirang (Arvind) Karandikar

[+91 96868 45700](tel:+919686845700)

[shrirang@algoasylum.com](mailto:shrirang@algoasylum.com)

<https://shrirang.karandikar.org>

## Profile

I have 20+ years of experience in engineering research and team management, driving innovation in a variety of different domains. I am adept at aligning technical strategy with organizational goals, mentoring diverse engineering teams, and delivering impactful solutions in complex, matrixed environments. I have a proven track record of leading cross-functional teams and managing large-scale projects with complex dependencies, leveraging data-driven decision-making to achieve operational excellence.

## Core Competencies

- **Technical Leadership:** Guided teams through end-to-end development of large-scale systems.
- **Program Management:** Expertise in driving cross-functional and cross-team projects, aligning strategies, and managing dependencies.
- **Automation & Optimization:** Developed scalable solutions and automated workflows to enhance efficiency.
- **People Management:** Extensive experience in coaching, mentoring, and leading global engineering teams.
- **Cross-Functional Collaboration:** Skilled in aligning strategy, processes, and priorities across diverse teams.

## Experience

### AlgoAsylum (2018 – Present) Founder

AlgoAsylum is a startup dedicated to revolutionizing education through innovative AI-driven techniques. I designed and developed the primary approach and initial implementation as a solo entrepreneur, showcasing end-to-end ownership of the product lifecycle. I was engaged in a funding round to scale the platform, but am currently transitioning the project as the rise of LLMs makes my approach redundant.

- Recognized as one of the first Emergent Ventures awardees for pioneering hyper-local pollution monitoring systems.
- Guided academic projects leveraging cloud infrastructure and associated services, focusing on automation and scalability.
- Mentored and collaborated with cross-functional teams on projects involving AI, HPC, and IoT.

### Shell India Markets Pvt. Ltd. (2012 – 2018) General Manager, Computational Technology

I managed a global team of 25 engineers and dozens of collaborators, overseeing strategic AI and HPC initiatives that included piloting HPC on the cloud and collaborating with external researchers on quantum computing. Working within Shell's highly matrixed organization, I successfully navigated complex relationships to align cross-functional teams with the company's broader vision.

- Set clear team goals and priorities, ensuring alignment with organizational objectives and delivering measurable results.
- Provided mentorship and career development for my team, significantly improving engagement and performance.

---

- Drove collaboration with external and internal stakeholders, fostering innovation across diverse teams and geographies.

#### **Computational Research Labs (2007 – 2012) Distinguished Scientist and Group Head**

CRL developed India's highest-ranked supercomputer, EKA, which reached #4 on the Top500 list. I was responsible, through a team of 30 engineers, for all research in hardware, software, and system design, with a focus on high-performance computing and efficient parallel algorithms.

- Supervised the development of scalable scientific algorithms for computational efficiency, enabling groundbreaking performance.
- Worked closely with external customers, ensuring that research outputs addressed commercial and technical needs.
- Collaborated with internal and external stakeholders to drive innovation, resulting in practical solutions and enhanced system designs.

#### **IBM Austin Research Labs (2005 – 2007) Research Staff Member**

- Developed the Electrical Violation Eliminator (EVE), an innovative solution for electrical correction that influenced IBM's physical design methodology.
- Authored five patents and contributed to advancements in buffering, gate sizing, and VLSI design optimization.
- Worked cross-functionally to integrate solutions into IBM's principal design tool, PDS, improving efficiency and accuracy.

#### **Intel Corporation (1997 – 1999) Component Design Engineer**

- Designed and optimized SHARK-FG, a fault simulator for multi-million transistor designs, significantly reducing testing time for Itanium microprocessors.
- Developed AutoCov, a genetic-programming-based tool for improving test coverage, enhancing the test suite for the Pentium-4 series.
- Collaborated with cross-functional teams to ensure the seamless integration of tools into larger design and testing ecosystems.

#### **Education**

- PhD in Electrical Engineering, University of Minnesota, 2004  
Synthesis and Performance Prediction of VLSI Designs.
- M.S. in Electrical Engineering, Clarkson University, 1996  
CAD Algorithms for VLSI Physical Design.
- B.E. in Electronics and Telecommunications, University of Pune, 1994

#### **Publications**

- 40+ publications in peer-reviewed journals and conferences.
- Multiple invited presentations at academic and industrial forums.
- 7 international patents granted.

